IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	09/347,106	Confirmation No.:	3360
First Named Inventor:	Hronik, Stanley A.	Filing Date:	July 2, 1999
Group Art Unit:	2186	Examiner:	Matthew Anderson
Atty. Docket No.:	M-7086 US		
Title:	Double Data Rate Synchronous SRAM with 100% Bus Utilization		
Assignee:	Integrated Device Technology, Inc.		

San Francisco, California
November 12, 2002

BOX NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir:

This paper is responsive to the non-final Office Action dated October 11, 2002. Applicant respectfully requests reconsideration of the Application in view of the following amendments and remarks.

IN THE CLAIMS

For the Examiner's convenience, a clean copy of all pending claims is presented below. Claim 52 is being amended to correct a minor typographical error. In accordance with 37 C.F.R. §1.121(c)(1)(ii), Attachment A provides a marked up version of the claim containing the change.

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1. A synchronous memory circuit comprising:

an address bus for receiving an address;